

## CLAIMS

1           1.     A method of recovering from ground bounce during a boundary  
2     scan test, said method comprising the step of operationally transitioning a  
3     Test Access Port controller from any of at least three undetermined controller  
4     states induced by the ground bounce to a determined controller state.

1           2     The method recited in claim 1 wherein the at least three  
2     undetermined controller states are selected from the group consisting of an  
3     UPDATE state, a RUN-TEST/IDLE state, a SELECT-DR-SCAN state, and a  
4     CAPTURE-DR state.

1           3.     The method recited in claim 2 wherein the at least three  
2     undetermined controller states are selected from the group consisting of an  
3     UPDATE state, a RUN-TEST/IDLE state, and a SELECT-DR-SCAN state.

1           4.     The method recited in claim 1 wherein the determined controller  
2     state is UPDATE-DR.

1           5.     The method recited in claim 1 wherein the at least three  
2     undetermined controller states includes four undetermined states selected

3 from the group consisting of an UPDATE state, a RUN-TEST/IDLE state, a  
4 SELECT-DR-SCAN state, and a CAPTURE-DR state.

1 6. The method recited in claim 1, wherein the controller  
2 transitioning step further comprises the step of providing a low Test Mode  
3 Select input to the TAP controller prior to a falling edge of a clock signal while  
4 in an UPDATE state.

1 7. The method recited in claim 6 wherein the controller  
2 transitioning step further comprises the step of providing the Test Access Port  
3 controller with a Test Mode Select input having the following bit pattern for a  
4 consecutive series of rising edges of clock pulses: a plurality of lows, high, a  
5 plurality of lows, high, high.

1 8. The method recited in claim 6 wherein the controller  
2 transitioning step further comprises the step of providing the Test Access Port  
3 with a Test Mode Select input having the following bit pattern for a  
4 consecutive series of clock rising edges of pulses: low, high, low, high, high.

1 9. A boundary scan apparatus with ground bounce recoverability  
2 comprising:  
3 at least one Test Access Port controller; and

4 means for operationally transitioning the Test Access Port  
5 controller from any of at least three undetermined controller states induced by  
6 the ground bounce to a determined controller state.

1 10. The apparatus recited in claim 9 wherein the controller state  
2 transitioning means comprises means for providing the Test Access Port  
3 controller with a low Test Mode Select input prior to a falling edge of a clock  
4 signal while in an update state.

1 11. The apparatus recited in claim 10 wherein the determined  
2 controller state is UPDATE-DR.

1 12. The apparatus recited in claim 11 wherein the at least three  
2 undetermined controller states are selected from the group consisting of an  
3 UPDATE state, a RUN-TEST/IDLE state, a SELECT-DR-SCAN state, and  
4 CAPTURE-DR state.

1 13. The apparatus recited in claim 12 wherein the at least three  
2 undetermined controller states are selected from the group consisting of an  
3 UPDATE state, a RUN-TEST/IDLE state, and SELECT-DR-SCAN state.

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1           14.    The apparatus recited in claim 12 wherein the at least three  
2   undetermined controller states are four undetermined controller states  
3   selected from the group consisting of an UPDATE state, a RUN-TEST/IDLE  
4   state, a SELECT-DR-SCAN state, and a CAPTURE-DR state.

1           15.    The apparatus recited in claim 14 wherein the controller state  
2   transitioning means comprises means for providing the Test Access Port  
3   controller with a Test Mode Select input having the following bit pattern for a  
4   consecutive series of rising edges of clock pulses: a plurality of lows, high, a  
5   plurality of lows, high, high.

1           16.    The apparatus recited in claim 13 wherein the controller state  
2   transitioning means comprises means for providing the Test Access Port with  
3   a Test Mode Select input having the following bit pattern for consecutive  
4   series of rising edges clock pulses: low, high, low, high, high.

1           17.    A boundary scan apparatus with ground bounce recoverability,  
2   comprising:  
3                an in-circuit tester configured to provide a Test Access Port  
4   controller with a low Test Mode Select input prior to a transition from an  
5   update state; and

6                   said in-circuit tester further configured to operationally transition  
7   the Test Access Port controller from any of at least four undetermined  
8   controller states induced by the ground bounce to an UPDATE-DR state.

1           18.    The apparatus recited in claim 17 wherein the at least four  
2   undetermined controller states are selected from the group consisting of an  
3   UPDATE state, RUN-TEST/IDLE, SELECT-DR-SCAN, and CAPTURE-DR.

1           19.    The apparatus recited in claim 17 wherein the in-circuit tester is  
2   further configured to provided the Test Access Port controller with a Test  
3   Mode Select input having the following bit pattern for a consecutive series of  
4   rising edges of clock pulses: a plurality of lows, high, a plurality of lows, high,  
5   high.

1           20.    The apparatus recited in claim 18 wherein the in-circuit tester is  
2   further configured to provided the Test Access Port controller with a Test  
3   Mode Select input having the following bit pattern for a consecutive series of  
4   rising edges of clock pulses: a plurality of lows, high, a plurality of lows, high,  
5   high.

1           21.    The apparatus recited in claim 17 wherein the in-circuit tester is  
2 further configured to operationally transition the Test Access Port controller  
3 from an undetermined data state to a determined data state.

1           22.    The apparatus recited in claim 21 wherein said data state  
2 transition begins when the Test Access Port controller has reached the  
3 UPDATE-DR state.

1           23.    The apparatus recited in claim 17 wherein the Test Access Port  
2 controller is one of a plurality of controllers in a boundary scan chain.

1           24.    The apparatus recited in claim 20 wherein the Test Access Port  
2 controller is one of a plurality of controllers in a boundary scan chain.

1           25.    The apparatus recited in claim 21 wherein the Test Access Port  
2 controller is one of a plurality of controllers in a boundary scan chain.

1           26.    The apparatus recited in claim 22 wherein the Test Access Port  
2 controller is one of a plurality of controllers in a boundary scan chain.